[**Control Sequencer**](https://www.youtube.com/watch?v=iVXcBfx2rIM&list=PLk4sSigu0N0W4v755N_O6Jk1WWrfWIGgm&index=9)**:**

The control sequencer either remember or erase the information on its input based on the logic in reset pin. Input is coming from the upper nibble of the Instruction register. This input is nothing but the opcode instructions.

**A diagram of a controller sequencer

Description automatically generated**

Halt pin stops the clock. In SAP-1 there are 6 T-States. But we built the controller sequencer using 6,5 & 4 T- States. If you don't understand the 5 & 4 T-States,  you can use 6 T-States. To reduce T-states, T1 that is address state, T2 that is increment state and T3 were combined.

**A diagram of a computer

Description automatically generated**

There is a Program Counter sub circuit inside which can count upto 7. There are 3 JK flip-flops inside of this circuit with modified inputs and outputs. Its negative edged trigerred. Counter will reset when it hits 6.

A screenshot of a computer

Description automatically generated